Session : Architecture and VLSI Hardware (II)

Time: 16:50 − 18:10

Chair:	*Ediz Cetin , University of Westminster*

C− BASED RAPID PROTOTYPING FOR DIGITAL SIGNAL PROCESSING (Abstract)

Bertrand Le Gal (LESTER Laboratory − UBS University, France)
Emmanuel Casseau (LESTER Laboratory − UBS University, France)
Sylvain Huet (LESTER Laboratory − UBS University, France)
Pierre Bomel (LESTER Laboratory − UBS University, France)
Christophe Jego (ENST Bretagne, France)
Eric Martin (LESTER Laboratory − UBS University, France)

Session : Architecture and VLSI Hardware (II)

Time: 16:50 − 18:10

Chair:	*Ediz Cetin , University of Westminster*

A DESIGN METHODOLOGY OF BUFFER−MEMORY ARCHITECTURES FOR FFT COMPUTATION (Abstract)

Chin−Liang Wang (National Tsing Hua University, Taiwan)
Sheng−Ju Ku (National Tsing Hua University, Taiwan)

A HIGH PERFORMANCE AND LOW POWER HARDWARE ARCHITECTURE FOR H.264 CAVLC ALGORITHM (Abstract)

Ilker Hamzaoglu (Sabanci University, Turkey)
Esra Sahin (Sabanci University, Turkey)

Session : Architecture and VLSI Hardware (II)

Time: 16:50 − 18:10

Chair:	*Ediz Cetin , University of Westminster*

A HIGH PERFORMANCE AND LOW COST HARDWARE ARCHITECTURE FOR H.264 TRANSFORM AND QUANTIZATION ALGORITHMS (Abstract)

Ilker Hamzaoglu (Sabanci University, Turkey)
Ozgur Tasdizen (Sabanci University, Turkey)

Back **Menu**