Session : Architecture and VLSI Hardware (I)

Time: 15:10 − 16:30

Chair:	*Levent Oktem , Synplicity Inc*

SYNDEX EXECUTIVE KERNELS FOR FAST DEVELOPMENT OF APPLICATIONS OVER HETEROGENEOUS ARCHITECTURES (Abstract)

Mickael Raulet (Mitsubishi Electric ITE, France)
Christophe Moy (IETR/Automatique & Communication Lab, France)
Fabrice Urban (IETR/Image group Lab, France)
Jean François Nezan (IETR/Image group Lab, France)
Olivier Deforges (IETR/Image group Lab, France)

Session : Architecture and VLSI Hardware (I)

Time: 15:10 − 16:30

Chair:	*Levent Oktem , Synplicity Inc*

NOVEL SYSTOLIC SCHEMES FOR SERIAL−PARALLEL MULTIPLICATION (Abstract)

Isidoros Sideris (Technical University Of Athens, Greece)
Kostantinos Anagnostopoulos (Technical University Of Athens, Greece)
Paraskevas Kalivas (Technical University Of Athens, Greece)
Kiamal Pekmestzi (Technical University Of Athens, Greece)

A PROGRAMMABLE SIMD−BASED MULTI−STANDARD RAKE RECEIVER ARCHITECTURE (Abstract)

Anders Nilsson (Linkoping University, Sweden)
Eric Tell (Linkoping University, Sweden)
Dake Liu (Linkoping University, Sweden)

Session : Architecture and VLSI Hardware (I)

Time: 15:10 − 16:30

Chair:	*Levent Oktem , Synplicity Inc*

A NOVEL, OPTIMIZED CORDIC CORE FOR PHASE CORRELATION MOTION ESTIMATION (Abstract)

Andrea Molino (Politecnico di Torino, Italy)
Fabrizio Vacca (Politecnico di Torino, Italy)

Back **Menu**