EFFICIENT FPGA IMPLEMENTATION OF AN ADAPTIVE IQ−IMBALANCE CORRECTOR FOR COMMUNICATION RECEIVERS USING REDUCED RANGE MULTIPLIERS (MonAmOR4)

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Abstract :

Digital signal processing techniques for compensating the IQ−imbalances in quadrature receivers are paving the path towards software−configurable−radio−receivers. Unsupervised signal processing algorithms operating at the baseband have been developed to deal with these impairments. This paper deals with an efficient FPGA implementation of an adaptive IQ−imbalance corrector using reduced range multipliers. Use of reduced−range multipliers result in 40% reduction in area and power consumption without a compromise in performance when compared with an efficiently designed general purpose multiplier approach.

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