



PARALLEL IMPLEMENTATION OF FINITE DIFFERENCE SCHEMES FOR THE PLATE EQUATION ON A FPGA-BASED MULTI-PROCESSOR ARRAY (MonPmOR11)



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✳ Abstract :

The computational complexity of the finite difference (FD) schemes for the solution of the plate equation prevents them from being used in musical applications. The explicit FD schemes can be parallelized to run on multi-processor arrays for achieving real-time performance. Field Programmable Gate Arrays (FPGAs) provide an ideal platform for implementing these architectures with the advantages of low-power and small form factor. The paper presents a design for implementing FD schemes for the plate equation on a multi-processor architecture on a FPGA device. The results show that 64 processing elements can be accommodated on a Xilinx X2VP50 device, achieving 487 kHz throughput for a square FD grid of 50x50 points.