100% OPERATIONAL EFFICIENT BIT−SERIAL PROGRAMMABLE FIR DIGITAL FILTERS (MonPmPO4)

Author(s) :

Paraskevas Kalivas (Technical University of Athens, Greece)
Andreas Tsirikos (Technical University of Athens, Greece)
Paul Bougas (Technical University of Athens, Greece)
Kiamal Pekmestzi (Technical University of Athens, Greece)

Abstract :

A new scheme for the implementation of programmable FIR digital filters with 100% operational efficiency is presented in this paper. The term 100% operational efficiency implies that no zero bits have to be inserted between successive in−put data words in order the filter input to be synchronized with the filter output. Both the input data and the filter out−put are in two's complement LSB−first bit−serial form. The coefficients are in two's complement bit−parallel form. All the intermediate results and the filter output are produced and handled in full precision. The proposed scheme is based on a special serial−parallel multiplier that operates with 100% efficiency. We exploit the internal registers and the free accumulation input in this multiplier to reduce the hardware complexity of the filter significantly. The proposed scheme is compared from the aspect of hardware complexity and efficiency with other bit−serial schemes.

Menu