



BIT-FLIPPING POST-PROCESSING FOR FORCED CONVERGENCE DECODING OF LDPC CODES (MonPmOR8)

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★ **Abstract :** The recently proposed forced convergence technique allows for reducing the decoding complexity of Low-Density Parity-Check Codes (LDPC) at only slight deterioration in performance. The basic idea is to restrict the message passing during LDPC decoding to the nodes that still significantly contribute to the decoding result. In this paper, we propose to add a bit-flipping post-processor to the forced convergence decoder in order to alleviate some problems of this novel technique, namely the error floors observed when aiming for high reduction in decoding complexity. Our results show that combining a hard decision bit-flipping with the forced convergence approach enables to almost retain original error correction performance while further reducing decoding complexity.