



A HIGH PERFORMANCE AND LOW POWER HARDWARE ARCHITECTURE FOR H.264 CAVLC ALGORITHM (ThuPmOR7)

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★ Abstract :

In this paper, we present a high performance and low power hardware architecture for real-time implementation of Context Adaptive Variable Length Coding (CAVLC) algorithm used in H.264 / MPEG4 Part 10 video coding standard. This hardware is designed to be used as part of a complete low power H.264 video coding system for portable applications. The proposed architecture is implemented in Verilog HDL. The Verilog RTL code is verified to work at 76 MHz in a Xilinx Virtex II FPGA and it is verified to work at 233 MHz in a 0.18 μ ASIC implementation. The FPGA and ASIC implementations can code 22 and 67 VGA frames (640x480) per second respectively.