PIPELINED MEMORY CONTROLLERS FOR DSP REAL−TIME APPLICATIONS HANDLING UNPREDICTABLE DATA ACCESSES (MonPmPO4)

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Abstract :

Abstract Multimedia applications such as video and image processing are often characterized by a large number of data accesses. In many digital signal−processing applications, the array access patterns are regular and periodic. In these cases, it becomes feasible and efficient to generate optimized Pipelined Memory Access Controllers. This technique is used to improve the pipeline access mode to RAM by creating specialized hardware components for generating addresses and packing and unpacking data items. In this paper we focus on the design, implementation and validation of external memory interfacing modules which can efficiently handle predictable address patterns as well as unpredictable (dynamic address computations) in a pipeline way. In a second time, we analyze the benefits of balancing dynamic address computation from datapath to dedicated units in the memory controller, optimizing bitwise of operators, and data locality (decreasing bus transfers for power efficient design).

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