A PROGRAMMABLE SIMD−BASED MULTI−STANDARD RAKE RECEIVER ARCHITECTURE (ThuPmOR4)

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Abstract :

Programmability with its associated flexibility will be increasingly important in future multi−standard radio systems. We are presenting a fully programmable and flexible DSP platform capable of efficiently performing channel estimation and MRC−based channel equalization for several CDMA based wireless transmission systems in software. Our processor is based on a DSP core with SIMD−computing clusters. We have mapped Rake receiver kernel−functions supporting several 3G standards to this micro−architecture and benchmarking shows that with the proposed instruction set architecture, our architecture can support channel estimation, equalization and decoding of: WCDMA FDD/TDD−modes and HSDPA at clock rate not exceeding 76 MHz during soft handover conditions.

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