PERFORMANCE EVALUATION OF FINE TIME SYNCHRONIZERS FOR WLANS (WedPmOR8)

Author(s) :

Maria Jose Canet (Universidad Politecnica de Valencia, Spain)
Vicenc Almenar (Universidad Politecnica de Valencia, Spain)
Javier Valls (Universidad Politecnica de Valencia, Spain)
Ian Wassel (University of Cambridge, United Kingdom)

Abstract :

In this paper the performance and implementation cost of three different fine time synchronization algorithms have been evaluated for their use in WLANs. In order to evaluate the performance, the residual time offset after fine time synchronization have been calculated. A hardware structure has been proposed for each algorithm and some simplifications are added that reduce the hardware cost without performance reduction. A Virtex II FPGA device has been selected as a target technology for the implementation. The results indicate that a cross−correlation algorithm with only 28 coefficients achieves the lowest hardware cost with similar performance with respect to the others algorithms.

Menu