A DESIGN METHODOLOGY OF BUFFER−MEMORY ARCHITECTURES FOR FFT COMPUTATION (ThuPmOR7)

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Abstract :

Memory−based architectures have received great attention for single−chip implementation of the fast Fourier transform (FFT). Basically, they can be roughly categorized as single−memory design, dual−memory design, and buffer−memory design. Among them, the buffer−memory design can balance the trade−off between memory size and control circuit complexity. In this paper, we present a design methodology of buffer−memory architectures for the radix−2 decimation−in−frequency FFT algorithm that can effectively reduce the needed memory. As compared to previous related works, the designs derived from the proposed methodology can reach the same throughput performance with a smaller memory size. These designs are rather attractive for long−length FFT applications, such as very−high−rate digital subscriber lines.

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